# \*\* Warning: (vsim-3008) C:/Users/liuya/Desktop/CPU\_Stage1/552\_Project/test/S18\_cpu\_testbench\_phase1.v(159): [CNNODP] - Component name (decode0) is not on a downward path.

# Time: 0 ns Iteration: 0 Instance: /cpu\_tb File: C:/Users/liuya/Desktop/CPU\_Stage1/552\_Project/test/S18\_cpu\_testbench\_phase1.v

# \*\* Error: (vsim-3043) C:/Users/liuya/Desktop/CPU\_Stage1/552\_Project/test/S18\_cpu\_testbench\_phase1.v(159): Unresolved reference to 'decode0' in DUT.decode0.

# Time: 0 ns Iteration: 0 Instance: /cpu\_tb File: C:/Users/liuya/Desktop/CPU\_Stage1/552\_Project/test/S18\_cpu\_testbench\_phase1.v

# \*\* Warning: (vsim-3008) C:/Users/liuya/Desktop/CPU\_Stage1/552\_Project/test/S18\_cpu\_testbench\_phase1.v(157): [CNNODP] - Component name (fetch0) is not on a downward path.

# Time: 0 ns Iteration: 0 Instance: /cpu\_tb File: C:/Users/liuya/Desktop/CPU\_Stage1/552\_Project/test/S18\_cpu\_testbench\_phase1.v

# \*\* Error: (vsim-3043) C:/Users/liuya/Desktop/CPU\_Stage1/552\_Project/test/S18\_cpu\_testbench\_phase1.v(157): Unresolved reference to 'fetch0' in DUT.fetch0.

# Time: 0 ns Iteration: 0 Instance: /cpu\_tb File: C:/Users/liuya/Desktop/CPU\_Stage1/552\_Project/test/S18\_cpu\_testbench\_phase1.v

# \*\* Warning: (vsim-3008) C:/Users/liuya/Desktop/CPU\_Stage1/552\_Project/test/S18\_cpu\_testbench\_phase1.v(168): [CNNODP] - Component name (memory0) is not on a downward path.

# Time: 0 ns Iteration: 0 Instance: /cpu\_tb File: C:/Users/liuya/Desktop/CPU\_Stage1/552\_Project/test/S18\_cpu\_testbench\_phase1.v

# \*\* Error: (vsim-3043) C:/Users/liuya/Desktop/CPU\_Stage1/552\_Project/test/S18\_cpu\_testbench\_phase1.v(168): Unresolved reference to 'memory0' in DUT.memory0.

# Time: 0 ns Iteration: 0 Instance: /cpu\_tb File: C:/Users/liuya/Desktop/CPU\_Stage1/552\_Project/test/S18\_cpu\_testbench\_phase1.v

# \*\* Error: (vsim-3063) C:/Users/liuya/Desktop/CPU\_Stage1/552\_Project/test/S18\_cpu\_testbench\_phase1.v(29): Port 'pc\_out' not found in the connected module (3rd connection).

# Time: 0 ns Iteration: 0 Instance: /cpu\_tb/DUT File: C:/Users/liuya/Desktop/CPU\_Stage1/552\_Project/cpu.v

# \*\* Warning: (vsim-3015) C:/Users/liuya/Desktop/CPU\_Stage1/552\_Project/cpu.v(101): [PCDPC] - Port size (16) does not match connection size (1) for port 'PC\_out'. The port definition is at: C:/Users/liuya/Desktop/CPU\_Stage1/552\_Project/PCctrl.v(1).

# Time: 0 ns Iteration: 0 Instance: /cpu\_tb/DUT/pc\_control File: C:/Users/liuya/Desktop/CPU\_Stage1/552\_Project/PCctrl.v

# \*\* Warning: (vsim-3015) C:/Users/liuya/Desktop/CPU\_Stage1/552\_Project/cpu.v(112): [PCDPC] - Port size (16) does not match connection size (15) for port 'data\_in'. The port definition is at: C:/Users/liuya/Desktop/CPU\_Stage1/552\_Project/memory.v(31).

# Time: 0 ns Iteration: 0 Instance: /cpu\_tb/DUT/instrucion\_mem File: C:/Users/liuya/Desktop/CPU\_Stage1/552\_Project/memory.v

# \*\* Warning: (vsim-3017) C:/Users/liuya/Desktop/CPU\_Stage1/552\_Project/cpu.v(123): [TFMPC] - Too few port connections. Expected 10, found 8.

# Time: 0 ns Iteration: 0 Instance: /cpu\_tb/DUT/control\_unit File: C:/Users/liuya/Desktop/CPU\_Stage1/552\_Project/Control.v

# \*\* Warning: (vsim-3722) C:/Users/liuya/Desktop/CPU\_Stage1/552\_Project/cpu.v(123): [TFMPC] - Missing connection for port 'ALUOp'.

# \*\* Warning: (vsim-3722) C:/Users/liuya/Desktop/CPU\_Stage1/552\_Project/cpu.v(123): [TFMPC] - Missing connection for port 'tophalf'.

# \*\* Warning: (vsim-3015) C:/Users/liuya/Desktop/CPU\_Stage1/552\_Project/cpu.v(159): [PCDPC] - Port size (3) does not match connection size (1) for port 'flag'. The port definition is at: C:/Users/liuya/Desktop/CPU\_Stage1/552\_Project/ALU.v(1).

# Time: 0 ns Iteration: 0 Instance: /cpu\_tb/DUT/alu File: C:/Users/liuya/Desktop/CPU\_Stage1/552\_Project/ALU.v

# \*\* Warning: (vsim-3015) C:/Users/liuya/Desktop/CPU\_Stage1/552\_Project/cpu.v(169): [PCDPC] - Port size (3) does not match connection size (1) for port 'flag\_new'. The port definition is at: C:/Users/liuya/Desktop/CPU\_Stage1/552\_Project/flag\_register.v(2).

# Time: 0 ns Iteration: 0 Instance: /cpu\_tb/DUT/flag\_reg File: C:/Users/liuya/Desktop/CPU\_Stage1/552\_Project/flag\_register.v

# \*\* Warning: (vsim-3015) C:/Users/liuya/Desktop/CPU\_Stage1/552\_Project/cpu.v(190): [PCDPC] - Port size (16) does not match connection size (32) for port 'B'. The port definition is at: C:/Users/liuya/Desktop/CPU\_Stage1/552\_Project/fulladders.v(77).

# Time: 0 ns Iteration: 0 Instance: /cpu\_tb/DUT/pcs\_adder File: C:/Users/liuya/Desktop/CPU\_Stage1/552\_Project/fulladders.v

# \*\* Error: (vsim-3063) C:/Users/liuya/Desktop/CPU\_Stage1/552\_Project/cpu.v(190): Port 'Cin' not found in the connected module (3rd connection).

# Time: 0 ns Iteration: 0 Instance: /cpu\_tb/DUT/pcs\_adder File: C:/Users/liuya/Desktop/CPU\_Stage1/552\_Project/fulladders.v

# \*\* Error: (vsim-3063) C:/Users/liuya/Desktop/CPU\_Stage1/552\_Project/cpu.v(190): Port 'Cout' not found in the connected module (5th connection).

# Time: 0 ns Iteration: 0 Instance: /cpu\_tb/DUT/pcs\_adder File: C:/Users/liuya/Desktop/CPU\_Stage1/552\_Project/fulladders.v

# \*\* Error: (vsim-3063) C:/Users/liuya/Desktop/CPU\_Stage1/552\_Project/fulladders.v(87): Port 'Sum' not found in the connected module (4th connection).

# Time: 0 ns Iteration: 0 Instance: /cpu\_tb/DUT/pcs\_adder/FA0 File: C:/Users/liuya/Desktop/CPU\_Stage1/552\_Project/fulladders.v

# \*\* Error: (vsim-3063) C:/Users/liuya/Desktop/CPU\_Stage1/552\_Project/fulladders.v(94): Port 'Sum' not found in the connected module (4th connection).

# Time: 0 ns Iteration: 0 Instance: /cpu\_tb/DUT/pcs\_adder/FA1 File: C:/Users/liuya/Desktop/CPU\_Stage1/552\_Project/fulladders.v

# \*\* Error: (vsim-3063) C:/Users/liuya/Desktop/CPU\_Stage1/552\_Project/fulladders.v(101): Port 'Sum' not found in the connected module (4th connection).

# Time: 0 ns Iteration: 0 Instance: /cpu\_tb/DUT/pcs\_adder/FA2 File: C:/Users/liuya/Desktop/CPU\_Stage1/552\_Project/fulladders.v

# \*\* Error: (vsim-3063) C:/Users/liuya/Desktop/CPU\_Stage1/552\_Project/fulladders.v(108): Port 'Sum' not found in the connected module (4th connection).

# Time: 0 ns Iteration: 0 Instance: /cpu\_tb/DUT/pcs\_adder/FA3 File: C:/Users/liuya/Desktop/CPU\_Stage1/552\_Project/fulladders.v